**Preset Eval\_DDR3\_x16 configuration:**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| SDRAM\_TYPE | = | DDR3 |  |
| PHYONLY | = | false |  |
| CLOCK\_DDR | = | 666 |  |
| CCC\_PLL\_CLOCK\_MULTIPLIER | = | 6 |  |
| CLOCK\_PLL\_REFERENCE | = | 111.000 |  |
| CLOCK\_RATE | = | 4 |  |
| CLOCK\_USER | = | 166.5 |  |
| MEMORY\_FORMAT | = | COMPONENT |  |
| WIDTH | = | 16 |  |
| SDRAM\_NB\_RANKS | = | 1 |  |
| ADDRESS\_MIRROR | = | false |  |
| DQ\_DQS\_GROUP\_SIZE | = | 8 |  |
| ROW\_ADDR\_WIDTH | = | 16 |  |
| COL\_ADDR\_WIDTH | = | 11 |  |
| BANK\_ADDR\_WIDTH | = | 3 |  |
| DM\_MODE | = | DM |  |
| ENABLE\_PAR\_ALERT | = | false |  |
| ENABLE\_ECC | = | false |  |
| SDRAM\_NUM\_CLK\_OUTS | = | 1 |  |
| READ\_BURST\_TYPE | = | SEQUENTIAL |  |
| BURST\_LENGTH | = | 0 |  |
| CAS\_LATENCY | = | 9 |  |
| RTT\_NOM | = | DISABLED |  |
| CAS\_ADDITIVE\_LATENCY | = | 0 |  |
| OUTPUT\_DRIVE\_STRENGTH | = | RZQ6 |  |
| SELF\_REFRESH\_TEMPERATURE | = | NORMAL |  |
| CAS\_WRITE\_LATENCY | = | 7 |  |
| PARTIAL\_ARRAY\_SELF\_REFRESH | = | FULL |  |
| RTT\_WR | = | OFF |  |
| TIMING\_RAS | = | 36 |  |
| TIMING\_RCD | = | 13.5 |  |
| TIMING\_RP | = | 13.5 |  |
| TIMING\_RC | = | 49.5 |  |
| TIMING\_WTR | = | 5 |  |
| TIMING\_REFI | = | 7.8 |  |
| TIMING\_RFC | = | 350 |  |
| TIMING\_WR | = | 15 |  |
| TIMING\_FAW | = | 30 |  |
| TIMING\_RRD | = | 7.5 |  |
| TIMING\_RTP | = | 7.5 |  |
| ZQ\_CAL\_INIT\_TIME | = | 512 |  |
| ZQ\_CALIB\_TYPE | = | 0 |  |
| ZQ\_CAL\_S\_TIME | = | 64 |  |
| ZQ\_CAL\_L\_TIME | = | 256 |  |
| ENABLE\_USER\_ZQCALIB | = | false |  |
| ZQ\_CALIB\_PERIOD | = | 200 |  |
| MEMCTRLR\_INST\_NO | = | 0 |  |
| FABRIC\_INTERFACE | = | AXI4 |  |
| AXI\_WIDTH | = | 64 |  |
| AXI\_ID\_WIDTH | = | 6 |  |
| USER\_POWER\_DOWN | = | false |  |
| ENABLE\_LOOKAHEAD\_PRECHARGE\_ACTIVATE | = | false |  |
| QUEUE\_DEPTH | = | 3 |  |
| USER\_SELF\_REFRESH | = | false |  |
| ADDRESS\_ORDERING | = | CHIP\_ROW\_BANK\_COL |  |
| ODT\_ENABLE\_WR\_RNK0\_ODT0 | = | true |  |
| ODT\_ENABLE\_WR\_RNK0\_ODT1 | = | false |  |
| ODT\_ENABLE\_WR\_RNK1\_ODT0 | = | false |  |
| ODT\_ENABLE\_WR\_RNK1\_ODT1 | = | true |  |
| ODT\_ENABLE\_RD\_RNK0\_ODT0 | = | false |  |
| ODT\_ENABLE\_RD\_RNK0\_ODT1 | = | false |  |
| ODT\_ENABLE\_RD\_RNK1\_ODT0 | = | false |  |
| ODT\_ENABLE\_RD\_RNK1\_ODT1 | = | false |  |
| ENABLE\_REINIT | = | false |  |
| SIMULATION\_MODE | = | FAST |  |